23. (Canceled)

24. (Canceled)

25. (Canceled)

26. (Currently Amended) A communications system, comprising:

a communications medium;

a processor with at least one processor line; and

a transceiver connected to the processor and to the communications medium, wherein the transceiver comprises a link level protocol, a driver including a driver output a driver circuit and an impedance control circuit, a canceller/equalizer, and a receiver including a receiver circuit and a bit deskew circuit;

wherein the link level protocol includes an ~~input, an output~~ input/output, a driver line and a receiver line;

wherein the driver is connected to the driver line, wherein the impedance control circuit includes an impedance control output connected to the driver circuit, and wherein the impedance control circuit modifies a driver output signal as a function of an external signal;

wherein the canceller/equalizer is connected to the driver line and the driver output, wherein the canceller/equalizer includes ~~an~~ a canceller/equalizer output, and wherein the canceller/equalizer generates a receive signal as a function of data on the driver line and the driver output; and

wherein the receiver is connected to the receiver line and the canceller/equalizer output, wherein the bit deskew circuit deskews signals from the receiver circuit as a function of a clock signal.

27. (Previously Presented) The communications system of claim 26 wherein the external signal is based on temperature of a resistive circuit.